UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,472	02/04/2004	Takaaki Sasaki	TAI 131 D1	1362

23995 7590 06/09/2005

RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
ZARNEKE, DAVID A	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/770,472	SASAKI, TAKAAKI	
	Examiner	Art Unit	
	David A. Zarneke	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102(b)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 14 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita et al., US Patent 5,726,493.

Yamashita teaches a method of fabricating a semiconductor package for three dimensional mounting comprising:

(a) placing a semiconductor chip [12] on an upper surface of a substrate [11], said substrate having the upper surface [11a] on which a first metal pattern (5, 21+) is formed and a lower surface [11b] on which a second metal pattern (5, 33+) is formed, said first metal pattern and second metal pattern being electrically connected to each other (using through holes [15]);

(b) electrically connecting the semiconductor chip and the first metal pattern to each other (using wires [14]);

(c) sealing the semiconductor chip and the first metal pattern with sealing resin [16]; and

(d) forming, in the sealing resin, a through hole which reaches the first metal pattern, and forming a wire [17] inside the through hole to electrically connect to the first metal pattern.

Regarding claim 18, Yamashita (figure 11) teaches: (a) disposing a second substrate [11] on the sealing resin after forming the wire inside the through hole; and (b) electrically

connecting the wire formed inside the through hole and a third metal pattern formed on the second substrate to each other (using solder balls 13).

Claims 16 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita et al., US Patent 5,726,493.

Yamashita teaches a method of fabricating a semiconductor package for three-dimensional mounting, comprising:

(a) preparing a substrate [11];

(b) forming a first metal pattern (5, 21+) on an upper surface [11a] of the substrate;

(c) forming a second metal pattern (5, 33+) on a lower surface [11b] of the substrate;

(d) electrically connecting the first metal pattern and the second metal pattern to each other (using through holes [15]);

(e) placing a semiconductor chip [12] on the upper surface of the substrate;

(f) electrically connecting the semiconductor chip and the first metal pattern to each other (using wires [14]);

(g) sealing the semiconductor chip and the first metal pattern with sealing resin [16];

(h) forming a through hole extending from the surface of the sealing resin to the first metal pattern (opening through which wire [17] is placed); and

(i) forming a wire [17] inside the through hole.

Regarding claim 21, Yamashita (figure 11) teaches: (a) disposing a second substrate [11] on the sealing resin after forming the wire inside the through hole; and (b) electrically connecting the wire formed inside the through hole and a third metal pattern formed on the second substrate to each other (using solder balls 13).

Claim Rejections - 35 USC § 102(e)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 14, 15, 18 and 19 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Farnworth et al., US Patent 6,451,624.

Farnworth (figure 5A) teaches a method of fabricating a semiconductor package for three dimensional mounting comprising:

(a) placing a semiconductor chip [14A] on an upper surface of a substrate [16A], said substrate having the upper surface [36A] on which a first metal pattern [22A] is formed and a lower surface [34A] on which a second metal pattern [22A] is formed, said first metal pattern and second metal pattern being electrically connected to each other (using through holes [15]);

(b) electrically connecting the semiconductor chip and the first metal pattern to each other [76A];

(c) sealing the semiconductor chip and the first metal pattern with sealing resin [20A]; and

(d) forming, in the sealing resin, a through hole [40A] which reaches the first metal pattern, and forming a wire [40A] inside the through hole to electrically connect to the first metal pattern.

Regarding claim 15, though Farnworth teaches the through hole is formed by irradiating a laser beam onto a predetermined position of the surface of the sealing resin (6, 11+).

With respect to claim 18, Farnworth (figure 8) teaches: (a) disposing a second substrate [10A-2-4] on the sealing resin after forming the wire inside the through hole; and (b) electrically connecting the wire formed inside the through hole and a third metal pattern formed on the second substrate to each other (using solder balls).

As to claim 19, Farnworth teaches placing a semiconductor chip includes placing a plurality of semiconductor chips on the upper surface of the substrate, the method further comprising: separating the plurality of semiconductor chips from each other to obtain a plurality of semiconductor packages after forming the wire inside the through hole (figures 6A-6G).

Claims 16, 17, 21 and 22 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Farnworth et al., US Patent 6,451,624.

Farnworth teaches a method of fabricating a semiconductor package for three-dimensional mounting, comprising:

(a) preparing a substrate [16A];

(b) forming a first metal pattern [22A] on an upper surface [36A] of the substrate;

(c) forming a second metal pattern [22A] on a lower surface [36A] of the substrate;

(d) electrically connecting the first metal pattern and the second metal pattern to each other;

(e) placing a semiconductor chip [14A] on the upper surface of the substrate;

(f) electrically connecting the semiconductor chip and the first metal pattern to each other (using wires [76A]);

(g) sealing the semiconductor chip and the first metal pattern with sealing resin [20A];

(h) forming a through hole extending from the surface of the sealing resin to the first metal pattern; and

(i) forming a wire [40A] inside the through hole.

Regarding claim 17, though Farnworth teaches the through hole is formed by irradiating a laser beam onto a predetermined position of the surface of the sealing resin (6, 11+).

With respect to claim 21, Farnworth (figure 8) teaches: (a) disposing a second substrate [10A-2-4] on the sealing resin after forming the wire inside the through hole; and (b) electrically connecting the wire formed inside the through hole and a third metal pattern formed on the second substrate to each other (using solder balls).

As to claim 22, Farnworth teaches placing a semiconductor chip includes placing a plurality of semiconductor chips on the upper surface of the substrate, the method further comprising: separating the plurality of semiconductor chips from each other to obtain a plurality of semiconductor packages after forming the wire inside the through hole (figures 6A-6G).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al., US Patent 5,726,493, as applied to claim 14 above.

Regarding claim 15, though Yamashita fails to teach the through hole is formed by irradiating a laser beam onto a predetermined position of the surface of the sealing resin, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a laser to form the through hole in the sealing resin because lasers are a conventionally known in the art method of forming openings in resins. The use of conventional methods to perform there known functions in a conventional process is obvious (MPEP 2144.07).

With respect to claim 19, though Yamashita fails to teach placing a semiconductor chip includes placing a plurality of semiconductor chips on the upper surface of the substrate, the method further comprising: separating the plurality of semiconductor chips from each other to obtain a plurality of semiconductor packages after forming the wire inside the through hole, the mere duplication of parts has no patentable significance unless a new and unexpected result is produced (In re Harza, 124 USPQ 378 (CCPA 1960)).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al., US Patent 5,726,493, or Farnworth et al., US Patent 6,451,624, as applied to claim 14 above, and further in view of Aiba, US Patent 6,348,728.

Yamashita and Farnworth both fail to teach: (a) forming a fourth wire on the surface of the sealing resin after forming the wire inside the through hole, the fourth wire being electrically connected to one end of the wire; (b) forming an insulating layer on the fourth wire; and (c) forming a third electrode which is electrically connected to the fourth wire and exposed from the insulating layer.

Aiba teaches semiconductor device comprising a redistribution layer (fourth wire) formed upon the surface of a sealing resin covering a chip, wherein a metal pattern (18a) is coated over a sealing resin (28), an insulating resin covers the metal pattern and lands (18b) [3rd electrode], which are electrically connected to the metal pattern (18a), are exposed there through (Figure 5B & 7, 51+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the redistribution layer of Aiba in the invention of Yamashita because redistribution layers (fourth wires) are conventionally known in the art and the use of conventional materials

to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962). Redistribution layers are commonly known in the art and are used to increase the mounting area of a semiconductor device to enable mounting to proceed using conventional techniques (Aiba, 1,66+).

Claims 17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al., US Patent 5,726,493, as applied to claim 16 above.

Regarding claim 17, though Yamashita fails to teach the through hole is formed by irradiating a laser beam onto a predetermined position of the surface of the sealing resin, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a laser to form the through hole in the sealing resin because lasers are a conventionally known in the art method of forming openings in resins. The use of conventional methods to perform there known functions in a conventional process is obvious (MPEP 2144.07).

With respect to claim 22, though Yamashita fails to teach placing a semiconductor chip includes placing a plurality of semiconductor chips on the upper surface of the substrate, the method further comprising: separating the plurality of semiconductor chips from each other to obtain a plurality of semiconductor packages after forming the wire inside the through hole, the mere duplication of parts has no patentable significance unless a new and unexpected result is produced (In re Harza, 124 USPQ 378 (CCPA 1960)).

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al., US Patent 5,726,493, or Farnworth et al., US Patent 6,451,624, as applied to claim 16 above, and further in view of Aiba, US Patent 6,348,728.

Yamashita and Farnworth both fail to teach: (a) forming a fourth wire on the surface of the sealing resin after forming the wire inside the through hole, the fourth wire being electrically connected to one end of the wire; (b) forming an insulating layer on the fourth wire; and (c) forming a third electrode which is electrically connected to the fourth wire and exposed from the insulating layer.

Aiba teaches semiconductor device comprising a redistribution layer (fourth wire) formed upon the surface of a sealing resin covering a chip, wherein a metal pattern (18a) is coated over a sealing resin (28), an insulating resin covers the metal pattern and lands (18b) [3rd electrode], which are electrically connected to the metal pattern (18a), are exposed there through (Figure 5B & 7, 51+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the redistribution layer of Aiba in the invention of Yamashita because redistribution layers (fourth wires) are conventionally known in the art and the use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962). Redistribution layers are commonly known in the art and are used to increase the mounting area of a semiconductor device to enable mounting to proceed using conventional techniques (Aiba, 1,66+).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-Th 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David A. Zarneke
Primary Examiner
June 6, 2005